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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,710	11/26/2003	Jean Charles Pina	SIG000102	7853
34399	7590	01/27/2006		
GARLICK HARRISON & MARKISON LLP P.O. BOX 160727 AUSTIN, TX 78716-0727			EXAMINER SONG, JASMINE	
			ART UNIT	PAPER NUMBER
			2188	

DATE MAILED: 01/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/723,710

Applicant(s)

PINA ET AL.

Examiner

Jasmine Song

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 and 12-20 is/are rejected.
- 7) ☒ Claim(s) 11 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Detailed Action

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

2. The drawings filed on 11/26/2003 have been approved by the Examiner.

Oath/Declaration

3. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-10 and 12-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Everett et al., US 6,220,510 B1.

Regarding claim 1, Everett teaches that a method comprising:

allocating a first portion (Fig.1, static data space 103) of a first memory (it is taught as an application abstract machine AAM) as a static section to store a main program (col.5, lines 49-53) which uses functional programs (it is taught as each application for every transaction, col.5, line 51-52 and col.3, lines 26-31) stored in a second memory (it is taught as IC card, col.3, lines 32-38);

allocating a second portion of the first memory as a dynamic section (Fig.1, second portion is taught as volatile such as RAM) to store other programs (it is taught as temporary data which is used much like conventional computer programs, col.6, lines 8-16), the dynamic section including an overlay space (it is taught as public segment) to overlay the functional programs loaded from the second memory (it is taught as the public segment contains the data passed between two applications or other data required or used by an application resident on the IC card; col.8, lines 23-29 and lines 33-37) to conserve memory capacity of the first memory (col.4, lines 53-63); and

allocating a third portion of the first memory (the delegate stack is preferably stored outside of an application's AAM memory space, this implies that the delegate can be stored inside of an application's AAM memory space) as a prelude space (it is taught as delegate stack) to store preludes which provide resource identifiers (it is taught as the delegator ID) to identify the functional programs to be loaded into the overlay space (col.10, lines 22-23 and lines 33-36), so that when the main program is to perform a functional operation without identifying a particular functional program stored in the second memory (it is taught as the identities of the delegated application can be

specifically called by the delegator application and without identifying a particular functional program; col.10, lines 36-41), a corresponding prelude in the prelude space for the functional operation provides a corresponding resource identifier to load a corresponding functional program into the overlay space (it is taught as each application has an delegator ID in the delegate stack to delegate a function to another delegated application stored on the IC card and perform the delegate request via the public memory space, col.10, lines 11-14 and lines 53-54).

Regarding claim 2, Everett teaches that the allocating of the prelude space allocates the prelude space in the static section of the first memory (Everett teaches that parameters are preferable stored at the top of public memory space, that implies that parameters can be stored at the static section which is non-volatile memory).

Regarding claim 3, Everett teaches that the allocating of the prelude space allocates the prelude space in the dynamic section of the first memory (col.8, last line to col.9, line 1).

Regarding claim 4, Everett teaches that the allocating of the dynamic section allocates the overlay space with a fixed entry address so that the preludes need not assign an address for loading the functional programs (col.8, lines 29-33).

Regarding claim 5, Everett teaches that the allocating of the first, second and third portions are allocated on the first memory resident on an integrated circuit (col.3, lines 64 to col.4, lines 6) and the functional programs to be loaded into the overlay space are resident on the second memory external to the integrated circuit (col.4, lines 17-20).

Regarding claim 6, Everett teaches that a method comprising:

- executing a program statement of a main program to perform a particular functional operation without identifying a corresponding functional program (it is taught as the identities of the delegated application can be specifically called by the delegator application and without identifying a particular functional program; col.10, lines 36-41);
- executing a prelude stored in a prelude space of a memory to provide a resource identifier for the functional operation (col.10, lines 6-32);
- using the resource identifier to identify a corresponding functional program to perform the particular functional operation (col.10, lines 36-41);
- loading the functional program into an overlay space allocated in the memory;

and executing the functional program in the overlay space (it is taught as each application has an delegator ID in the delegate stack to delegate a function to another delegated application stored on the IC card and perform the delegate request via the public memory space, col.10, lines 11-14 and lines 53-54).

Regarding claim 7, Everett teaches that the loading the functional program into the overlay space loads the functional program into a fixed entry address so that an address to load the functional program need not be specified in the prelude (col.8, lines 29-33).

Regarding claim 8, Everett teaches that executing the prelude loads the resource identifier into a register (it is taught as load the delegator ID to the delegate stack) and transfers execution to a routine to call the functional program (col.10, lines 34-39).

Regarding claim 9, Everett teaches that using the resource identifier includes reading the resource identifier in the register by the routine to call the functional program (col.10, lines 34-39).

Regarding claim 10, Everett teaches that further comprising returning to the main program after executing the functional program in the overlay space (Fig.4, it is taught as performing a return delegation control command by the delegate application, col.10, lines 55-67).

Regarding claim 12, Everett teaches that an apparatus comprising:
a first memory (it is taught as an application abstract machine AAM) having a first portion (Fig.1, static data space 103) as a static section to store a main program (col.5, lines 49-53) which uses functional programs (it is taught as each application for every

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transaction, col.5, line 51-52 and col.3, lines 26-31), a second portion as a dynamic section (Fig.1, second portion is taught as volatile such as RAM) to store other programs which reside in the first memory for a shorter duration than the main program (it is taught as temporary data which is used much like conventional computer programs, col.6, lines 8-16), and a prelude space (it is taught as delegate stack) to store preludes which provide resource identifiers (it is taught as the delegator ID) to identify the functional programs to be loaded into an overlay space (col.10, lines 22-23 and lines 33-36) located within the dynamic section (col.8, last line to col.9, line 1); and a second memory (it is taught as IC card, col.3, lines 32-38) operably coupled to store the functional programs and to transfer a particular functional program into the overlay space (col.10, lines 22-23 and lines 33-36 and col.10, lines 53-54) when the main program performs a functional operation without identifying the particular functional program stored in the second memory (it is taught as the identities of the delegated application can be specifically called by the delegator application and without identifying a particular functional program; col.10, lines 36-41), but in which a corresponding prelude in the prelude space for the functional operation provides a corresponding resource identifier to identify the particular functional program to be loaded into the overlay space (it is taught as each application has an delegator ID in the delegate stack to delegate a function to another delegated application stored on the IC card and perform the delegate request via the public memory space, col.10, lines 11-14 and lines 53-54).

Regarding claims 13 and 17, Everett teaches that the first memory is a random access memory resident in an integrated circuit (it is taught as RAM within AAM) and the second memory is an external memory to the integrated circuit (it is taught as IC flash card, col.4, lines 53-58).

Regarding claims 14 and 18, Everett teaches that the second memory is larger in capacity than the first memory (col.4, lines 7-17), but in which the functional programs are loaded into the overlay space to allow overlay in use of the functional programs (col.4, lines 17-20).

Regarding claims 15 and 19, Everett teaches that the overlay space has a fixed entry address so that an address to load functional programs need not be specified in the preludes (col.8, lines 29-33).

Regarding claim 16, Everett teaches that a multi-function handheld device comprising:

a system on a chip integrated circuit that includes an internal memory (it is taught as an application abstract machine AAM) arranged to have a first portion (Fig.1, static data space 103) as a static section to store a main program (col.5, lines 49-53) which uses functional programs (it is taught as each application for every transaction, col.5, line 51-52 and col.3, lines 26-31), a second portion as a dynamic section (Fig.1, second portion is taught as volatile such as RAM) to store other programs which reside in the

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internal memory for a shorter duration than the main program (it is taught as temporary data which is used much like conventional computer programs, col.6, lines 8-16), and a prelude space (it is taught as delegate stack) to store preludes which provide resource identifiers (it is taught as the delegator ID) to identify the functional programs to be loaded into an overlay space (col.10, lines 22-23 and lines 33-36) located within the dynamic section (col.8, last line to col.9, line 1), the overlay space to have a fixed entry address (col.8, lines 29-33); and

an external memory (it is taught as IC card, col.3, lines 32-38) operably coupled to the integrated circuit to store the functional programs and to transfer a particular functional program into the overlay space (col.10, lines 22-23 and lines 33-36 and col.10, lines 53-54) when the main program performs a functional operation without identifying the particular functional program (it is taught as the identities of the delegated application can be specifically called by the delegator application and without identifying a particular functional program; col.10, lines 36-41).

Regarding claim 20, Everett teaches that the integrated circuit includes a register for the preludes to load resource identifiers (it is taught as load the delegator ID to the delegate stack), which are to be used by a calling routine to load the functional programs (col.10, lines 34-39).

Allowable Subject Matter

6. Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

8. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 571-272-4213. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone numbers for the organization where this application or proceeding is assigned are 571-273-8300.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Jasmine Song



Patent Examiner

January 20, 2006

FOR

Mano Padmanabhan

Supervisory Patent Examiner

Technology Center 2100



GARY PORTKA
PRIMARY EXAMINER